WHAT IS CLAIMED IS:

1. A trench capacitor for use in a semiconductor memory cell, the capacitor comprising:

a trench formed in a semiconductor substrate;

a first and second conducting capacitor plate each located in said trench;

a dielectric layer located between said first and second capacitor plates, as a capacitor dielectric;

an isolation collar in an upper region of said trench; and

an optional conducting filling material, filled into the trench;

wherein said dielectric layer has been applied by one of an ALD, ALCVD, and CVD method.

2. The trench capacitor as claimed in claim 1, wherein said first capacitor plate is a region of increased doping in the semiconductor substrate in a lower region of said trench and said second capacitor plate is said conducting filling material.

3. A trench capacitor for use in a semiconductor memory cell, the trench capacitor comprising:

a trench formed in a semiconductor substrate;

a first and a second conducting capacitor plate, located in said trench;

a dielectric layer, located between said first and said second capacitor plates, as the capacitor dielectric;

an isolation collar in an upper region of the trench; and

an optional conducting filling material in said trench;

wherein:

said first capacitor plate is a region of increased doping in the semiconductor substrate in a lower region of the trench; and

a first metal electrode layer is provided on said dielectric layer inside said trench as said second capacitor plate.

4. The trench capacitor as claimed in claim 3, wherein a second metal electrode layer is provided in the upper region of said trench and is in electrical connection with said first metal electrode layer, and said second metal electrode layer optionally fills the upper trench region.

5. A trench capacitor for use in a semiconductor memory cell, the capacitor comprising:

a trench formed in a semiconductor substrate;

a first and a second conducting capacitor plate located in said trench;

a dielectric layer located between said first and said second capacitor plates, as a capacitor dielectric;

an isolation collar in an upper region of said trench; and

an optional conducting filling material, filled in said trench;

wherein:

a third metal electrode layer is provided between said dielectric layer and the

semiconductor substrate as said first capacitor plate; and

a fourth metal electrode layer is provided on the other side of said dielectric layer as said second capacitor plate.

6. The trench capacitor as claimed in claim 5, wherein:

a second metal electrode layer is provided in the upper region of the trench and is in electrical connection with said fourth metal electrode layer; and

said second metal electrode layer optionally fills the upper trench region.

7. The trench capacitor as claimed in claim 5, wherein said dielectric layer and said fourth metal electrode layer are led into a region of said isolation collar.

8. The trench capacitor as claimed in claim 7, wherein said third metal electrode layer is led into the region of said isolation collar.

9. The trench capacitor as claimed in claim 3, wherein one of said first metal electrode layer, second metal electrode layer, third metal electrode layer, fourth metal electrode layer and said dielectric layer have been applied by one of an ALD, ALCVD and CVD methods.

10. The trench capacitor as claimed in claim 3, wherein one of said first, second third and fourth metal electrode layers comprises at least one of the following materials: TiN, WN, TaN, HfN, ZrN, Ti, W, Ta, Si, TaSiN, WSiN, TiAlN, WSi, MoSi and CoSi.

11. The trench capacitor as claimed in claim 1, wherein said trench has a lower widened region.

12. The trench capacitor as claimed in claim 1, wherein said dielectric layer comprises at least one of the following materials:

$A1_2O_3$, Ta_2O_5, ZrO_2, HfO_2, Y_2O_3, La_2O_3, TiO_2; Al-Ta-O, Al-Zr-O, Al-Hf-O, Al-La-O, Al-Ti-O, Zr-Y-O, Zr-Si-O, Hf-Si-O, Si-O-N, Ta-O-N, Gd_2O_3, SNO_3, La-Si-O, Ti-Si-O, $LaA1O_3$, $ZrTiO_4$, (Zr, Sn)TiO_4, $SrZrO_4$, $LaA1O_4$ and $BaZrO_3$.

13. The trench capacitor as claimed in claim 1, wherein said conducting filling material is composed of a first conducting filling layer in a lower trench region and a second conducting filling layer in the upper trench region.

14. A method for producing a trench capacitor, for use in a semiconductor memory cell, the method comprising:

forming a trench in a semiconductor substrate;

providing a first and a second conducting capacitor plate in the trench;

providing a dielectric layer as a capacitor dielectric between the first and the second capacitor plates;

forming an isolation collar in an upper region of the trench;

optionally filling a conducting filling material into the trench; and

applying the dielectric layer by one of an ALD, ALCVD and CVD method.

15. A method for producing a trench capacitor for use in a semiconductor memory cell, comprising:

forming a trench in a semiconductor substrate;

providing a first and a second conducting capacitor plate;

providing a dielectric layer as a capacitor dielectric between the first and the second capacitor plates;

forming an isolation collar in an upper region of the trench;

optionally filling the trench with a conducting filling material; and

providing a first metal electrode layer on the dielectric layer inside the trench as the second capacitor plate.

16. The method as claimed in claim 15, further comprising wherein a second metal electrode layer is provided in the upper region of the trench and is in electrical connection with the first metal electrode layer.

17. A method for producing a trench capacitor for use in a semiconductor memory cell, the method comprising:

forming a trench in a semiconductor substrate;

providing a first and a second conducting capacitor plate in the trench;

providing a dielectric layer as the capacitor dielectric, between the first and the second capacitor plates;

forming an isolation collar in an upper region of the trench;

optionally filling a conducting filling material into the trench;

providing a third metal electrode layer between the dielectric layer and the semiconductor substrate as the first capacitor plate; and

providing a fourth metal electrode layer on the other side of the dielectric layer as the second capacitor plate.

18. The method as claimed in claim 17, further comprising providing a second metal electrode layer between the isolation collar and the conducting filling material in the upper region of the trench, wherein the second metal electrode layer is in electrical connection with the fourth metal electrode layer.

19. The method as claimed in claim 17, further comprising leading the dielectric layer and the fourth metal electrode layer into a region of the isolation collar.

20. The method as claimed in claim 19, further comprising leading the third metal electrode layer into a region of the isolation collar.

21. The method as claimed in claim 16, further comprising applying one of the first metal electrode layer, second metal electrode layer, third metal electrode layer, fourth metal electrode layer and the dielectric layer, by one of an ALD, ALCVD, and CVD method.